Contact Information

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Career Goal

To use my technical and leadership abilities to solve problems for the benefit of society by creatively and positively developing disruptive technology in algorithm development and high-performance/evolutionary computation/AI.

Professional Experience

2018-Present Sr. Deep Learning SW Engineer at Intel Corp./Movidius , Dublin, Ireland

Coded binary file serializer for NCE HW accelerator and SW processor back-ends to MyriadX chip. Developed python and bash tools for inference accuracy testing on HW. Wrote compiler passes for FP16, fixed-point numeric accuracy optimizations on Neural Compute Engine (NCE) (CNN HW accelerator). Contributed to technical due-diligence during Vertex.ai acquisition by reviewing code, running benchmarks, recreating results from open source libraries. Used gtest, github, c++, cmake, bash, python, PlaidML, Ubuntu VM on windows, slack, Movidius MDK.

2016-2017 Contract SW Engineer at Intel Corp., Hillsboro, OR

Worked on all levels of SW stack for DLIA SW product. Created and trained CNN models in caffe/c++ and tensorflow/python. Prepared MNIST and Caltech101 data sets for training including writing perl scripts to label, organize data. Designed, coded and tested algorithms for conversion of prototxt models into FPGA compliant compute graphs. (reformat maxpool and convolution layers to fit FPGA IP) . Designed and coded memory buffer management / tensor re-order algorithms in middle layers (mkldnn). Wrote tests using Alexnet, googlenet, VGG16, caffenet, custom topologies and imagenet classification data set. Designed and coded product installer scripts: created RPM, debian, pip and docker installation files. Use of CentOS and ubuntu linux, vi, makefiles, bazel, Perforce, git.

2013-2015 Consulting Engineer/ Scientist at Intractus Research LLC, Hillsboro, OR

Founded start-up company to provide services to clients interested in applying signal processing and machine learning algorithms towards the solution of intractable problems. Handle business affairs of company such as meeting lawyer, accountant handling LLC affairs, payroll, budget, taxes etc. Contact prospective clients to sell services.

Successfully developed 2D to 3D video conversion and autostereoscopic rendering algorithms for client VEFXi Corp. (15 month contract successfully completed) Coded object oriented java to prototype algorithms and worked with FPGA designers on HW implementation. Designed and coded multi-threaded, evolutionary algorithms running on a server compute cluster that I specified and assembled. Designed/coded/used image processing and machine learning techniques including artificial neural nets, genetic algorithms, FIR filters, decimation, compression, pattern detection, FFT/DCT, motion estimation, fixed point DSP math, various

color spaces and media representation standards. Several patents being filed related to real time 3D video/image depth estimation and auto-stereoscopic rendering.

Currently I am developing a MLaaS application on the google app-engine. I am coding with HTML, java, python and GWT in eclipse IDE on an Ubuntu linux workstation that I put together. Also using JDO to interface with the google datastore.

2007-2013 Sr. Electrical Engineer at Rockwell Collins in Wilsonville, OR.

Lead Electrical Engineer on multiple Head-Up Display (HUD) development programs. Lead teams of 5-10 engineers developing new image processing FPGAs and circuit card designs to DO-254 DAL-A process (FAA safety critical systems). Provided technical leadership to reporting engineers and cross-functional program team. Contributed to project plans, system safety analyses, and requirements definition. Presented at customer design reviews. Assisted qualification testing to DO-160 parameters (military specifications). Responsible for establishing and meeting cost and schedule targets for electrical engineering team. Pioneered use of new tools for verification of complex FPGAs, and drove innovative design features such as use of compression techniques during distortion image processing to eliminate need for external RAM buffering of video data. Familiar with DVI, QDRII SRAM, Xilinx Virtex FPGAs, VHDL, System-Verilog, Mentor EDA tools/methods, SAP earned value management.

2001-2007 High School Mathematics Teacher for Hillsboro School District.

Earned masters degree in education and endorsements to teach high school math and physics. Full-time classroom teacher at Century HS and Hillsboro HS. Taught classes up to International Baccalaureate Calculus and Advanced Placement Physics. Successful personal and professional interaction with students, parents and administrators. . I feel many science and engineering professionals, and their communities, would benefit if more of us shared our passion, philosophy and skill by devoting part of our careers toward the education of young people

1983-2001 18 years at Intel, Oregon and San Diego. Wide range of responsibilities:

1999-2001, Staff Engineer leading design and planning of new products including Intel's first Infiniband switch, and wireless LAN product in San Diego, CA. Lead development teams, wrote architecture spec's. Employed by XLNT Corp. until purchase by Intel was finalized. US Patent: "Enhanced Configuration of Infiniband Links". Worked closely with marketing, engineering and management teams on new product definition and goals. Had 1:1 meeting with Intel CEO Paul Otellini while preparing for Infiniband kick-off conference. Familiar with successfully navigating Intel's new product development process.

1996-1998, Validation Engineer in microprocessor division. Invented, deployed novel random component verification schemes while earning masters degree. Unix, perl and C++ programming. Lead team of Jr. engineers. Knowledge of Intel chipsets/busses. US Patent: "Codec with Genetic Adaptation." IEEE Publication: "Maximizing Functional Test Coverage in ASICs Using Evolutionary Algorithms." Et al. Wrote perl scripts to utilize several hundred IBM Unix workstations across the company to perform massively parallel machine learning and functional verification simulations of new chip designs. Presented at Intel Innovators Conference in Folsom, CA.

1990-1996 Sr. Design Engineer in supercomputer systems division. Lead Design Engineer on multiple circuit cards for iWarp, Paragon, and other teraflops systems such as ASCI Red.

Designed DRAM, Gbit serial IO, VME I/F, PLD's, PCI master, slave, arbiter for Pentium Paragon system. Printed circuit board design, customer interaction, VHDL, synthesis, 1GHz GaAs SERDES, JTAG, Altera and Xilinx FPGA's. Mentor V8 design tools. HW emulation of ASIC designs with FPGAs. Designed CPU card for world's first teraflop level supercomputer. Met often with CAD tool and programmable logic device vendors on tool flows, feature bugs, training, etc.

1983-1990 Various design/test engineering positions at Intel Corporation in Hillsboro, OR. PC motherboard design. US. Patent on DRAM control. 80386/486 CPU bus, Worked on the in-circuit emulator for the 386 chip which was critical in Intel winning the IBM PC business. Programmed Teradyne Automated Test Equipment (ATE). Attained security clearance for work on military microcontroller firmware project.

1981-1983 Computer Programmer at Michigan Kidney Registry. I worked with medical staff and administrators developing medical records analysis programs and data entry GUIs, in FORTRAN, while a student at the University of Michigan. I worked 20 hours per week during the school year and 40 hours during the summer. I made enough money doing this for 2 years to pay for my own college tuition. Proficient in use of IBM 370 mainframe system including IBM-370 assembler.

Education

MS Electrical Engineering, Columbia University, New York , NY Feb'99

Concentration: Telecommunications/signal processing
Advisor: Dr. A. Eleftheriadis (MPEG committee member).

Perfect 800/800 score on GRE math exam. Elective graduate courses in information theory, complexity theory, optimization methods in finance and stochastic processes. Wrote novel data compression tool in C++ with related performance analysis and research paper as part of masters thesis/project. Used custom image/video file formatting tools developed by Columbia University researchers. Transcript available.

MA Teaching/Education, Pacific University ,Forest Grove, OR May'03.

Oregon TSPC license to teach secondary level advanced math and physics.
(passed subject matter exams and background check.)

BS Computer Engineering, University of Michigan, Ann Arbor, MI. May'83

Concentration: Computer components and sub-systems

Additional elective courses in physics and linear algebra. Initially majored in Physics before transferring to the engineering school. Transcript available.

6/79 Univ. of Detroit Jesuit High school Class valedictorian GPA=4.0

Computer Skills

Most fluent in java, C++, perl and VHDL. Comfortable using any appropriate computer language. Have successfully coded and/or lead big projects using Pascal, FORTRAN, BASIC, IBM mainframe and Intel microprocessor assembly languages, HTML, Tcl, any many other special purpose coding languages such as System Verilog.

Often the level of computer sophistication associated with the projects I have been working require my teams to invent our own computer languages and databases, such as for controlling new/custom electronic hardware or HW/SW interfaces such as for test case generation. I think the language used is less important than a well-structured design of the objects and algorithms reflecting an understanding of the problem to be solved.

I have designed and programmed massively parallel computer systems for many years. I have experience designing and coding multi-threaded and multi-process applications in java, perl and C++ on Unix and Windows operating systems. I designed parts of, and made tests for, several of Intel's tera-scale, Unix based, supercomputers.

I have used the following basic productivity tools extensively:
-MS Office suite (Word, Excel, Powerpoint)
-Version control tools (Subversion/SVN, Tortoise, Git)

I have mentored an award-winning student (Intel international science fair) doing a genomics research science-fair project which involved writing statistics and pattern detection algorithms in perl to analyze FASTA/ASCII format nucleotide sequence files downloaded from the NCBI GenBank database.

Leadership Skills

Formal training and extensive use of DO-254/DO-178B code development process for complex aviation systems. (required for FAA certification). Including project planning, requirements definition, system design, implementation, verification, validation and documentation on multiple, safety critical, FAA certified avionics systems.

Other skills/training:
-SAP earned value management system
-IBM PREP database (also multiple other business-related databases)
-Time management/SMART goal setting
-Efficient meetings
-Constructive confrontation

I have received excellent feedback as a group leader at Rockwell Collins and Intel. I take pride in the fact that my teams are focused and efficient, due to strong goal orientation and meaningful communication practices. I tend to call a lot of meetings but only with a strong agenda. I required formal weekly status and goal setting communication among the teams I have led. I rely heavily on established processes and best practices, with an eye for continual improvement.

The wide range of positions I have held in industry and education has given me a unique background to interact positively with a wide range a people. (students, doctors, lawyers, engineers, scientists, managers, administrators, investors, customers, clients, etc.)

Patents and Publications

Codec with genetic adaptation

Patent number: 6539366

Abstract: A codec to compress information by generating a set of basis vectors based upon a population of vectors according to a pseudo-random sequence; and encoding the information into a set of coefficients indicative of a projection of the information onto the linear span of the set of basis vectors provided the projection satisfies a criterion of goodness. The generation of the basis vectors is based upon a genetic algorithm. To decode, the information is reconstructed or uncompressed by summing the set of basis vectors weighted by the set of coefficients.

Type: Grant

Filed: April 30, 1998

Issued: March 25, 2003

Assignee: Intel Corporation

Inventors: Patrick F. Doyle, Burcin Aktan

Memory address decoder with storage for memory attribute information

Patent number: 5353431

Abstract: A programmable and testable memory address decoder for a computer system where a static random access memory device is used to store memory configuration information.

Type: Grant

Filed: February 8, 1994

Issued: October 4, 1994

Assignee: Intel Corporation

Inventors: Patrick F. Doyle, Leonard W. Cross, Roger Noar

Enhanced configuration of infiniband links

Publication number	US20030018761 A1
Publication type:	Application
Application number	US 09/752,369
Publication date	Jan 23, 2003
Filing date	Dec 29, 2000
Priority date	Dec 29, 2000
Inventors	Patrick Doyle, Nelson Ge
Original Assignee	Patrick Doyle, Nelson Ge

3D System Including Additional 2D to 3D Conversion

Patent application number: 15/293,565

Filed: October 14, 2016

Inventors: Craig Peterson, Sergey Lomov, Lee Newbill, Bob McCormick, Manual Muro, Pat Doyle and Markus Roberts

3D System Including a Neural Network

Patent application number: 15/293,5382

Filed: October 14, 2016

Inventors: Craig Peterson, Pat Doyle, Markus Roberts, and Sergey Lomov

Maximizing functional test coverage in ASICs using evolutionary algorithms

IEEE CONFERENCE PUBLICATIONS 2001

Authors: **Burcin Aktan**, Patrick F. Doyle, Garrison Greenwood, **Molly Shor**

Personal Information

Born	7/25/1961 in Highland Park MI
Citizenship	USA
Gender	Male

Interests

Alpine skiing
Physical fitness, jogging, swimming, biking, weight training
Quantum physics, quantum computation
Computer vision, machine learning
Cognitive Science, Neuroscience
Philosophy of science, Information theory
Time with family
Financial investments